Bel Canto Design

DAC2

24/192 Up-sampling DAC

Technical White Paper

The CD audio channel was developed based on the Nyquist sampling theorem which states that sampling at 2x the highest frequency of interest will allow the recreation of all information up to that frequency. The last 20+ years of technical development has resulted in a recording and playback channel which now approaches Nyquist's limits. The DAC2 from Bel Canto proves the point. It also proves that the CD channel can be a very satisfying musical source, comparable with any current alternative.

The goal of the DAC2 processor development was to use the latest technical developments to improve on the performance of the DAC1. All critical performance criteria were addressed in the new DAC2 design. Lessons learned from the DAC1 development were applied along with the best of the latest technologies available to provide higher levels of measured and musical performance.

Performance enhancements were achieved in the following areas:

1) Timing jitter in the DAC clock.
2) Quantization and Sample Rate Converter noise in the Digital to Analog conversion process.
3) Time domain smearing.
4) Electromagnetic Interference (EMI) distortion sources.

Advances in integrated DAC, DSP, Digital Filter, Analog processing and PC board layout techniques have allowed us to substantially and audibly improve on all four of these critical performance areas.

1) Timing jitter in the DAC clock

Timing jitter in the clock used to convert the digital signal to the analog domain is known to cause measurable and audible degradation of the analog signal. The typical digital signal processing architecture and the SPDIF serial data interface uses a Voltage Controlled Oscillator (VCO) within a Phase Lock Loop (PLL) architecture to generate the clock used for converting the digital data to an analog signal. This architecture is shown below in Figure 1.
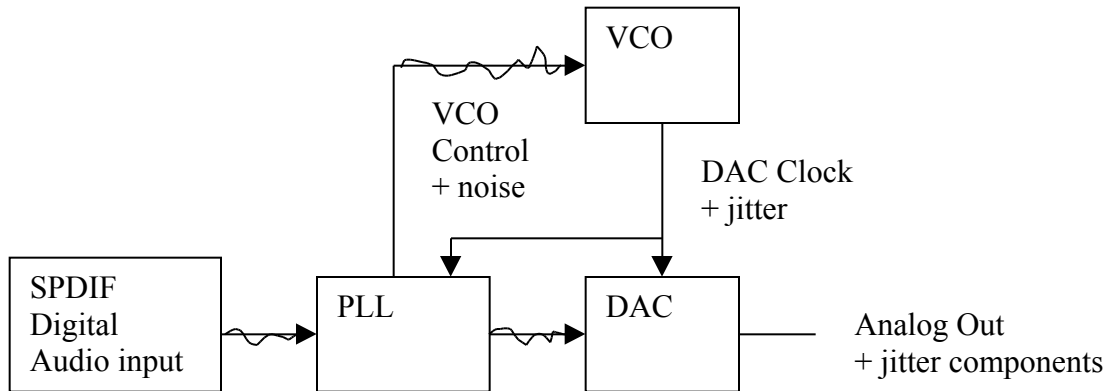
Figure 1. Typical digital audio interface architecture.

This architecture uses the PLL to determine the clock frequency needed to convert the digital audio data to an analog signal. The VCO is an oscillator, or clock, whose frequency of oscillation is controllable through the VCO control line. This control line is driven by the PLL so that the DAC Clock follows the clock frequency of the incoming digital audio data. Jitter is an instantaneous change in the clock frequency. Jitter on the DAC clock is caused by variation of the VCO control line and is an expected result of the PLL process. A filter associated with the PLL can reduce variation of the VCO control line but the fact remains that this is effectively an open window to the introduction of all types of clock jitter to the DAC clock. Including effects from various digital cables, CD players, de-jitter boxes, etc. Various techniques to reduce the amount of clock jitter have been tried, including FIFO buffers to increase the PLL filter's effectiveness, and the use of Voltage Controlled Crystal Oscillators (VCXO) in an attempt to create a fundamentally more stable clock. All of these techniques are only incremental improvements in a flawed approach.

A better approach to generating a truly jitter free DAC clock is shown in Figure 2.
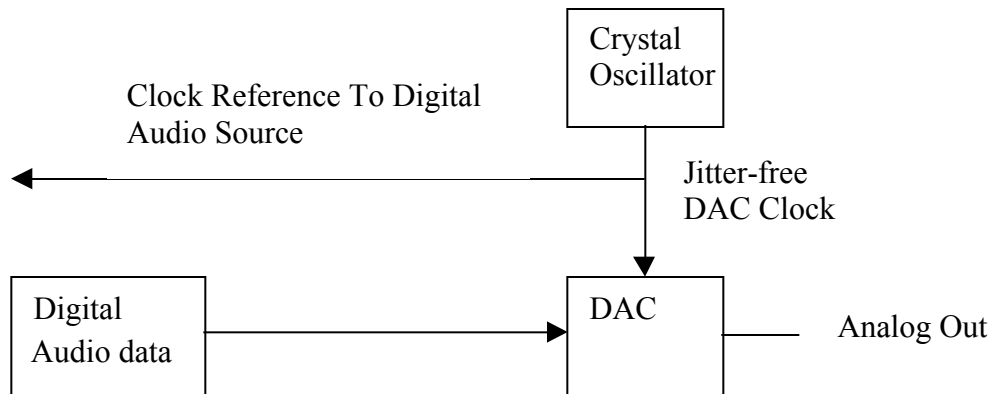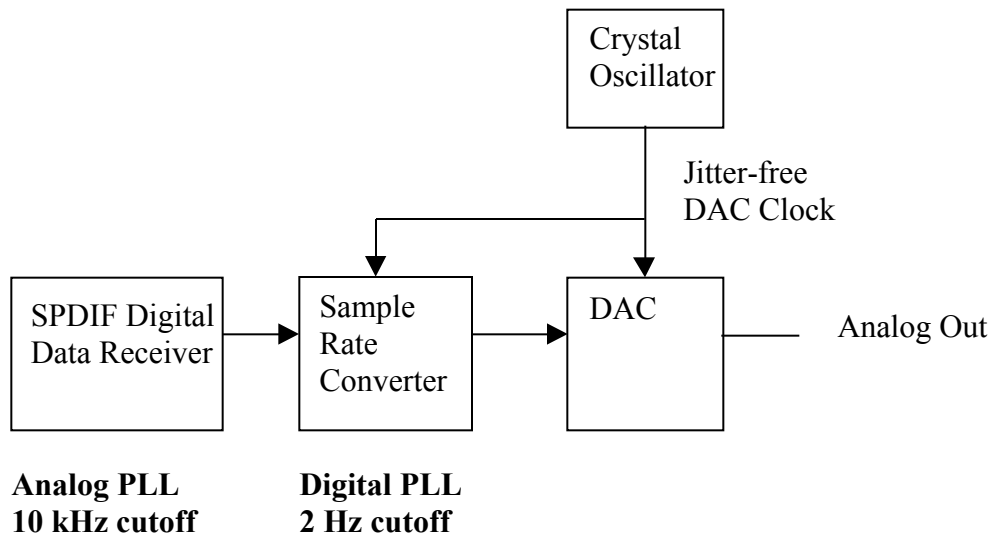
Figure 2. Isolated DAC clock.

In this circuit a very stable Crystal Oscillator is used for the DAC clock with no control input to change the clock frequency. This clock is sent back to the digital source where it is used to control the digital audio data sent to the DAC. This approach removes the VCO and its control port, which is a window for jitter to enter the DAC clock. This approach has been used in high priced converters and implementations of the IIS interface and can work very well. It's problems are related to the fact that it does not adhere to the SPDIF format and requires a custom and expensive transport, DAC and additional connections between the digital source and DAC.

The input of the Bel Canto DAC2 consists of a SPDIF Receiver and analog PLL feeding a new Asynchronous Sample Rate Converter (ASRC) using the clock architecture of Figure 3 within a standard SPDIF format. This maintains full compatibility with all SPDIF digital sources including low cost CD and DVD players. The DAC clock in the DAC2 is a local Crystal Oscillator driving the Digital Filter/DAC directly. A buffered clock output from the Digital Filter is sent back to the input sample rate converter circuit where it is compared digitally to the incoming data, setting internal registers for calculating the precise relationship between the incoming SPDIF data and the DAC clock. There is no VCO control port where jitter can enter and the DAC conversion is performed in a jitter-free environment.

The DAC2 adds to the jitter rejection performance of the DAC1 by using a dual PLL architecture to reject any jitter components above 2 Hz. This dual architecture provides the cleanest possible clock environment for the data conversion process.

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                                    ┌──────────────┐
                                    │  Crystal     │
                                    │  Oscillator  │
                                    └──────┬───────┘
                                           │  Jitter-free
                                           │  DAC Clock
                   ┌───────────┐           │
                   ▼           ▼           ▼
┌──────────────┐  ┌────────────┐  ┌──────────┐
│ SPDIF Digital│  │ Sample     │  │ DAC      │──────── Analog Out
│ Data Receiver│──│ Rate       │──│          │
│              │  │ Converter  │  │          │
└──────────────┘  └────────────┘  └──────────┘
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Analog PLL   **Digital PLL**
10 kHz cutoff   **2 Hz cutoff**

Figure 3. Bel Canto DAC 2 Enhanced Zero-jitter SPDIF interface uses dual analog and digital PLL architecture to further remove jitter components from effecting the analog output.

2) Quantization noise and distortion residue in the Asynchronous Sample Rate Conversion and Digital to Analog conversion process.

The new **Asynchronous Sample Rate Converter used in the DAC2 provides a minimum 139 dB of dynamic range under all conversion modes**. This represents at least a 20 dB improvement over previous SRC devices. This insures that any filter residue from the sample rate conversion process is well below the thermal noise floor of the DAC. The new dual differential DAC used in the DAC2 provides 117dB of dynamic range capability and insures that any quantization residue at the DAC output is well below the noise floor of the original recording.

An advanced, **True Differential Current to Voltage** (TDIV) converter circuit is used at the DAC output. This circuit is extremely low noise, low distortion and fast. It has a bandwidth over 100 MHz to insure that no inter-modulation distortion components are generated at this critical point in the conversion process. Performance is further enhanced by using high speed, ultra high precision 0.1% resistors in the critical I/V conversion and analog filter stages.

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3) Time domain smearing.

A substantial audible degradation occurs in most CD playback because of the digital brick wall filters used in most processors. These brick wall filters introduce a time smearing effect on transient information. This is illustrated in
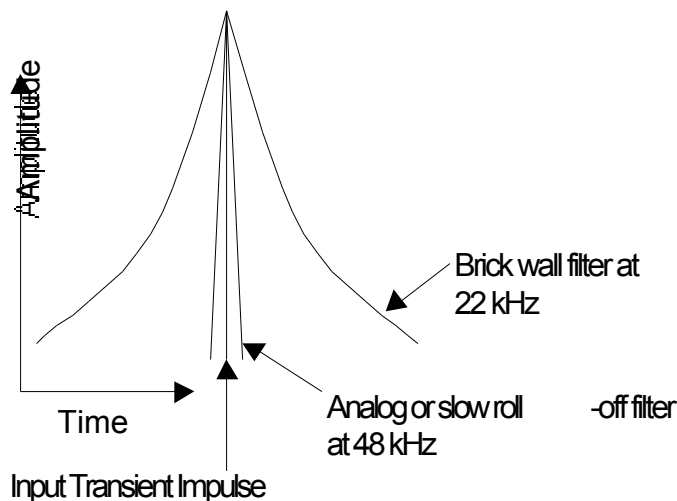Figure 4.

Figure 4. Time/Amplitude impulse response of different filter types.

As shown in figure 4, a typical gentle filter response, such as a moving coil cartridge rolling off at 48 kHz or a slow roll-off digital filter at 96 kHz has a tight response to a transient with only very slight, inaudible, smearing. A brick wall digital filter, used in virtually all CD processors at 22 kHz, spreads the low level signal energy over a much larger time, reducing imaging accuracy adding a grainy quality to the high frequencies and decreasing the sense of space and ease in a recording. The DAC2 processes all inputs using a 96 kHz, slow roll-off digital filter. This provides analog-like energy response without the 20 kHz frequency response droop that slow roll-off filters incur when used at 22 kHz. Many of the advantages of 24/96 or 24/192 recording have been due to the reduction of time smear.

4) Electromagnetic Interference (EMI) distortion sources.

EMI is caused by high frequency signals being radiated and picked up by other circuits where these signals cause distortion or interference. DAC processors, especially when used at 192 kHz with over-sampling filters, can be serious sources of EMI. This results in interference with FM radios and distortion of analog audio sources, including the DAC outputs and phono preamplifier stages. EMI problems start with the unwanted radiation of high frequency clocks and data signals. Radiation requires an antenna, which is any unshielded wire of sufficient length. The use of the latest DSP and DAC technologies permits us to package the DAC2 in an extremely tight space and reduced power, reducing critical clock and data line lengths to fractions of an inch. This approach, combined with a **4-layer circuit board**, isolated analog and digital ground planes

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and multiple stages of power supply with LC filters insures that EMI is even lower than on the DAC1. This provides the least interference with the DAC analog output stages or any other sensitive analog signals. A further benefit of this approach is that the entire DAC and analog and digital power supplies fit within a 3 by 8 inch board and can be placed anywhere in the system, including within preamplifier, integrated amp or surround processor devices. Indeed, as technology improves it becomes obvious that smaller can often be better.

Sample Rate Converter Primer

A new Asynchronous Sample Rate Converter (ASRC) has been mentioned in this white paper and is critical to the performance of the DAC2. ASRC is a digital signal processing technique which uses digital filters to change the sample rate of a digital audio signal from, for example, 44.1 kHz to 192 kHz. The ASRC in the DAC2 is a new device designed to reduce residual noise products of this conversion to more than 139 dB below maximum output. This level is more than 40 dB below the noise floor of all 16 bit recordings and is even below the noise floor of all analog recordings and 24/96 sources. When processing 24/192 material the residue from the SRC is more than 139 dB down, below the thermal noise floor of the best d/acs. All of the advantages of doing sample rate conversion described above are realized without an increase in noise or distortion from the SRC process. This custom DSP IC uses the latest technology operating with 32 bit precision and the equivalent processing capability of a powerful microprocessor.

Summary

By focussing the latest and best technologies and audio design practices the DAC2 allows all digital music sources to be reproduced with virtually no DAC related errors. It is remarkable how good 16/44.1 material can sound. The DAC2 proves once and for all that Nyquist was right all along…. With the advent of new digital technologies like SACD and DVD-A the DAC2 is a device which is most relevant in insuring the viability and musical enjoyment of the millions of CD recordings available today.

While the DAC2 is not the first of the 24/192 d/acs available, Bel Canto has waited until the a superior solution could be engineered using the best and latest technologies. We are certain that you will agree that it has been worth the effort.