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Dac3 White Paper

Design Goal

The design goal for the Dac3 was to set a new standard for digital audio playback components through the application of technical advances in Digital to Analog Conversion devices and design techniques in a product that can function as:

- An Audio Digital to Analog Conversion processor with levels of objective and subjective audio performance that set a New Standard in the market
- A Digital Preamplifier with Volume control
- A Primary Digital Audio source component for traditional CD playback sources and computer based sources

These Dac3 goals where to be achieved through the application and use of optimum solutions for:

- Digital Audio Receiver architecture
- Digital Audio Asynchronous Sample Rate Converters
- Digital to Analog Conversion and Filter devices with near 24 bit analog performance
- Class A balanced I/V and analog output stage electronics
- Carefully Chosen analog passive devices
- Optimized multi-layer, isolated analog and digital PC board layout techniques
- Optimized low noise analog and isolated digital broad-band power supply technologies
- Stable, Low Noise, Ultra-Clock ^{tm} circuit
- RoHS Compliance

The goal of designing the Dac3 to be a New Standard in digital audio conversion has been met with the unique combination of solutions called out above. Details of these solutions will be described below.

Digital Audio Receiver Architecture

We found in our development that complete galvanic isolation for all digital audio inputs was necessary to achieve the extremely low noise that our design goals required. Digital audio source noise would otherwise couple into the processor and compromise the performance of the analog outputs. We used wide-bandwidth shielded input transformers for all electrical digital inputs; even the USB input is coupled through a transformer to

insure that the noisy computer environment does not compromise the Dac3 performance. Care in the layout of the digital input board was required to maintain the required isolation from ground noise across a wide bandwidth.

The digital inputs are then AC coupled into the latest SPDIF receiver IC. Again, great care in PC board layout and power supply architecture insure that the receiver operates optimally, achieving good jitter rejection in this initial analog Phase Lock Loop (PLL) function. Jitter levels of 200 picoseconds are obtained at this point in the circuit. The USB input has an additional level of jitter rejection to deal with the noisy signals coming off of typical computer-based audio sources.

Digital Audio Asynchronous Sample Rate Conversion (ASRC)

The next stage in the Dac3 architecture uses the latest generation of ASRC. This digital processor and filter provides 2 critical functions:

- Sample rate conversion to 24bit/192KHz audio signals using linear phase interpolation filters
- Digital PLL function for superior jitter rejection

The first function is achieved with an internal digital dynamic range capability of 170dB. This extreme dynamic range insures that the interpolation process does not inject any spurious signals or noise into the output signal. The interpolation process also uses a linear phase filter. This preserves the waveform shape and prevents phase errors from skewing harmonic relationships in the audio signals.

The Digital PLL function is necessary to insure that the Ultra-Clock internal to the Dac3 is not corrupted by jitter in the data stream. Our measurements show that this second PLL stage prevents even high levels of incoming jitter (10 nanoseconds p-p at 10 KHz) from corrupting the analog output of the Dac3. This is even more remarkable given the very low inherent noise floor of the Dac3. Without this Digital PLL the Dac3 would be susceptible to incoming jitter, with easily measured intermodulation components due to jitter. These comparison results can be seen in Figures 1 and 2.

Digital Audio Conversion and Filter and Analog Output Section

The Dac3 uses the latest generation of DAC device, the PCM1792A. This device provides the advantages of both multi-bit and delta sigma DAC architectures and achieves 130 dB of analog dynamic range in the Dac3. The slow roll-off linear phase filter used also provides that last degree of sonic naturalness to the audio output, further reducing any phase errors in the upper octaves of the harmonic structure of the audio signal.

This DAC uses a dual differential current output architecture. We use a balanced current to voltage (I/V) conversion stage using Class A biased high speed, low noise amplifiers. The amplifiers use a single gain stage in a folded cascode architecture with 90 MHz of bandwidth to insure the lowest possible noise and distortion in this most critical of analog stages. A single pole filter at nearly 100 KHz insures that the linear phase digital filters are not compromised in the analog output. The final balanced analog output stage uses a fully Class A biased balanced amplifier, also using a folded cascade architecture. All passive devices in the analog section are chosen for optimum measured and sonic performance.

The combination of the PCM1792A and our proprietary Class A analog output stage achieves nearly 24 bits of analog performance capability. This performance essentially eliminates issues related to quantization noise from the D/A conversion and allows uncompromised use of the digital level control.

PC Board Layout Techniques and Power Supply Architecture

The single largest and most critical passive device in any circuit design is the PC board. Optimum layout techniques are used using 4-layer PC board structure to insure that both analog and digital circuit domains operate in the best possible environment. Multiple ground planes and power planes are used to keep the multiple power and ground domains optimally isolated and maintain low noise over a very wide bandwidth. Indeed, using this approach the PC board itself functions as the final decoupling capacitor for the circuitry. The use of the latest large scale IC devices allows the Dac3 board design to be quite compact, further reducing noise levels and insuring that critical signal paths are short and quiet.

Separate isolated power transformers are used for the analog and digital power domains. Multiple-stage regulation, low noise, high-speed schottky rectifiers and audio grade decoupling capacitors for the analog stages are used extensively. Critical analog power supplies use extremely low noise regulators locally to insure optimum power for these wide dynamic range circuits.

Stable, Low Noise Ultra-Clock ^{tm}

Finally, the foundation of the Dac3 rests on a new ultra low noise Master Clock device. This device uses advanced clock synthesis and DSP filtering techniques to achieve remarkably accurate and stable clock specifications. Frequency accuracy of 0.0001% and jitter specifications of 1 picoseconds RMS or 5 picoseconds Peak to Peak are 50 to 100 times better than the best alternative clock devices. Care in locating and routing the critical clock lines and the low noise power supply architecture insure that the advantages of the Ultra-Clock ^{tm} are realized in the final analog output. The Ultra-Clock ^{tm} brings the subjective performance of the Dac3 to new levels of musical realism. The solid

foundation gives the Dac3's sonic performance an organic quality that evokes the best of pure analog playback systems.

Digital Preamplifier Functionality

The Dac3 has a 4.5Vrms balanced output that is designed to optimally drive a power amplifier directly. The wide dynamic range with output noise that is some 15 dB lower than the best analog preamplifiers allows digital domain volume control to be used. This volume control technique removes any vestige of the analog volume control, keeping the analog signal path as short as possible. The clean noise floor of the Dac3 and the dither applied to the 24 bit internal signal insure that the digital level control remains transparent. There is literally no compromise in controlling the audio signal through the Dac3.

RoHS Compliance

The Dac3 represents one of the first high performance audio products to comply with the new RoHS standards. All soldering is done using Tin/Silver Eutectic. This is better for both the environment and for the sonic performance of the Dac3.

Conclusion

The Dac3 has actually gone beyond our original expectations, achieving performance levels that we only dreamed could be possible for digital audio playback. The Dac3 sets new standards for an audio source component.

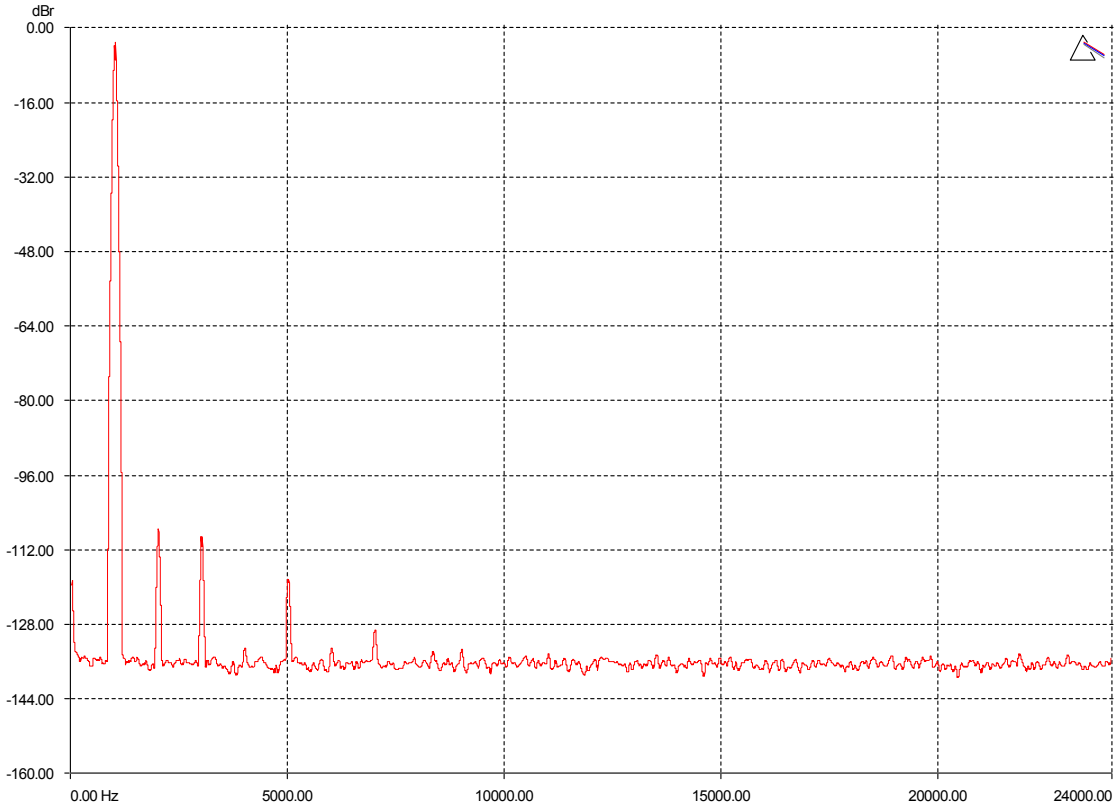

Figure 1. Dac3 0dB 1KHz Sine, no jitter on input data.

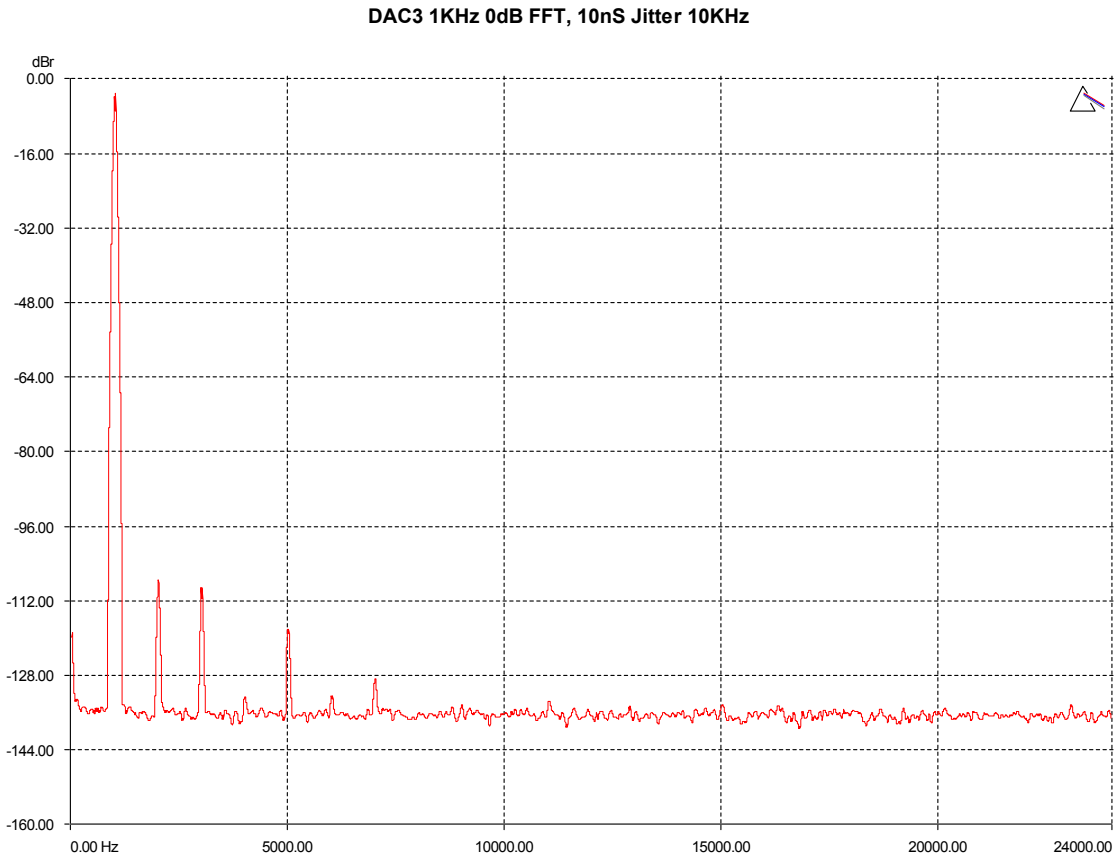

Figure 2. Dac3 0dB 1KHz Sine, 10nS jitter at 10KHz on input data.

Note that there is no presence of any spikes from the jitter around 10KHz. Indeed the plot is as clean as the plot with no jitter on the input signal.

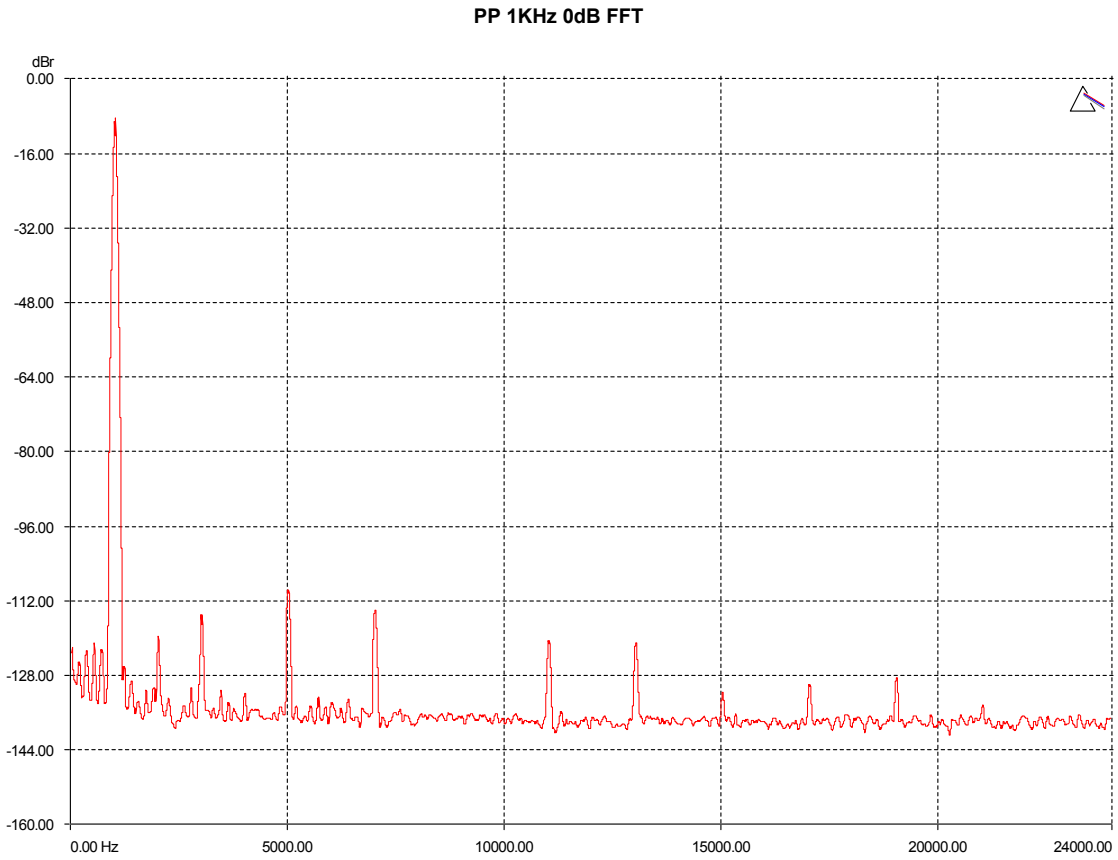

Figure 3. Single stage PLL DAC 1KHz 0dB, no jitter (Other DAC product)

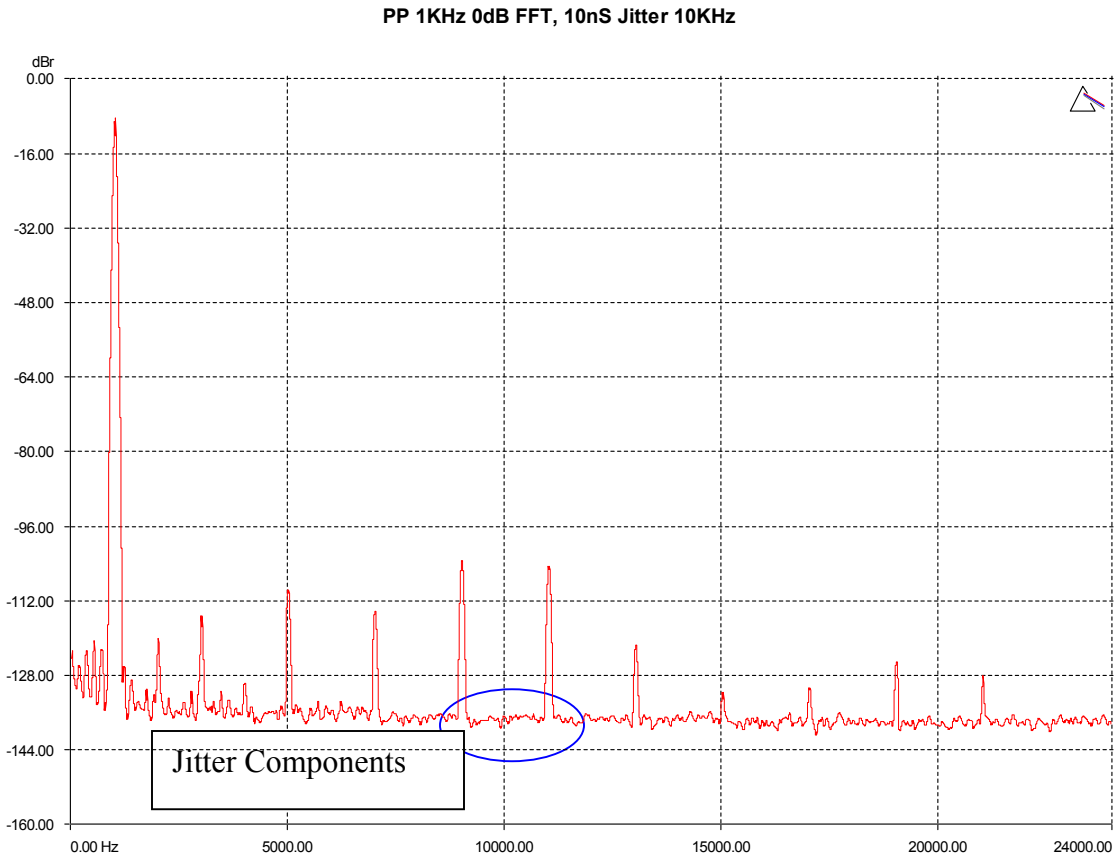

Figure 4. Single Stage PLL DAC 1KHz 0dB 10nS jitter at 10KHz. (Other DAC product)

Note the additional spikes at 9KHz and 11KHz, these are due to the added jitter on the input.

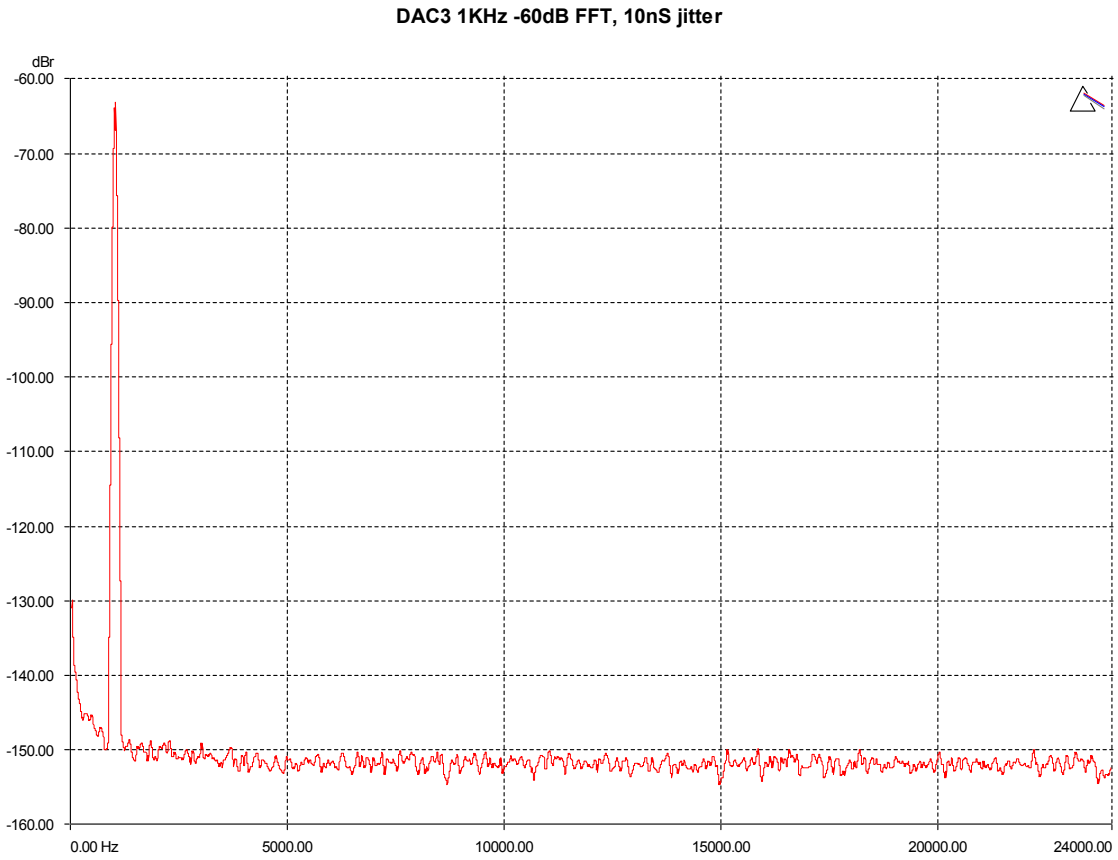

Figure 5. Dac3 1KHz input at –60dB with 10nS jitter.

Note how clean the noise floor is in this plot, no distortion or noise components are present with this noise floor at –150dB.

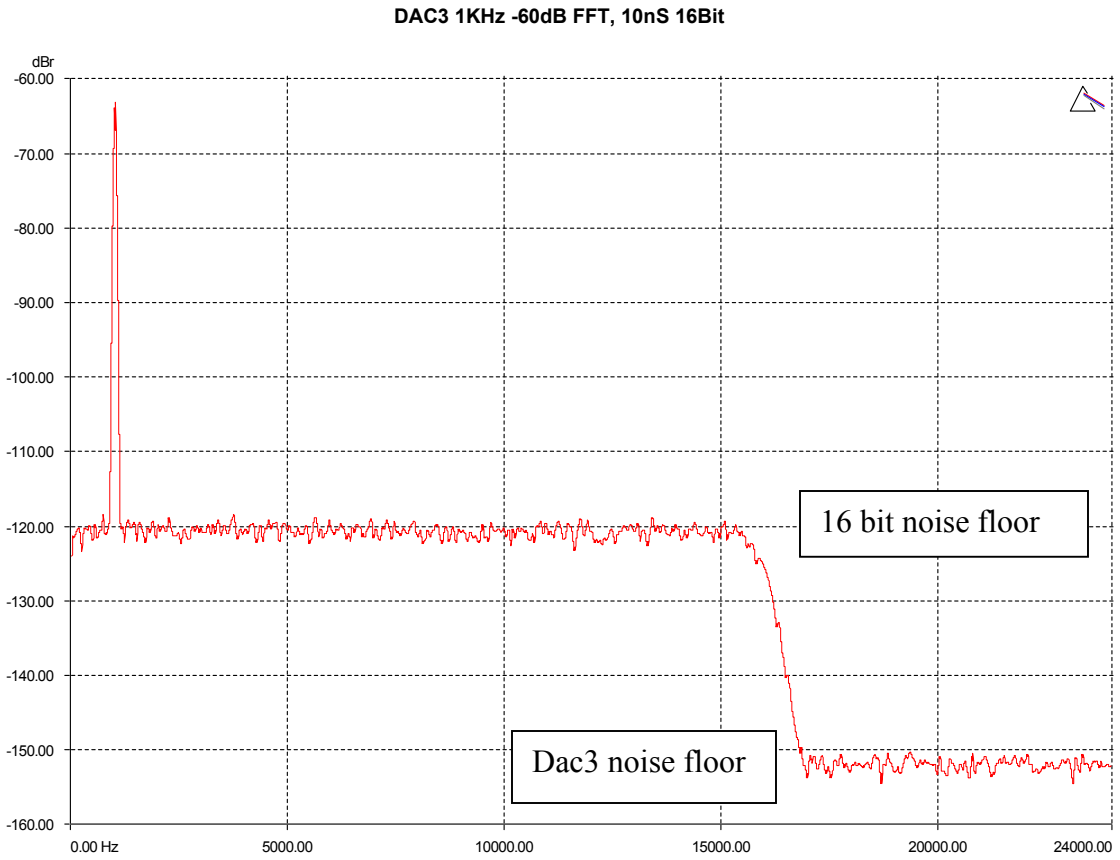

Figure 6. This shows the relative noise floor of the Dac3 versus a 16 bit input signal at 32 KS/s with a roll-off at 16 KHz. Note that the Dac3 noise floor is over 30dB lower than the 16 bit signal.